Express Mail Label No. EL696074627US 10-02-00 A

09/29/00 JC632 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. F-316
Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD AND APPARATUS FOR RAPID DATA TRANFER BETWEEN DIS-SIMILAR DEVICES

and invented by:

Stan W. BOWLIN

09/676974 JC836 U.S. PTO 09/29/00

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **9 (nine)** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets **2 (two)**
   b. ☐ Informal Number of Sheets
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☒ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☒ Certificate of Mailing
    ☐ First Class ☒ Express Mail *(Specify Label No.)*: **EL696074627US**

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. F-316
Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☒ Additional Enclosures *(please identify below):*

Inventor Information Sheet (Patent Bibliographical Data)

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	9	- 20 =	0	x	$18.00	$0.00
Indep. Claims	3	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)*						$0.00
					TOTAL FILING FEE	$690.00

☒ A check in the amount of **$690.00** to cover the filing fee is enclosed.

☐ The Commissioner is hereby authorized to charge and credit Deposit Account No. as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
- ☐ Credit any overpayment.
- ☐ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: **September 29, 2000**

James H. Walters, Reg. No. 35,731
DELLETT AND WALTERS
310 S.W. Fourth Avenue, Suite 1101
Portland, Oregon 97204
(503) 224-0115

cc:

CERTIFICATE OF MAILING BY "EXPRESS MAIL" (37 CFR 1.10) Applicant(s): **Stan W. BOWLIN**			Docket No. **F-316**
Serial No.	Filing Date	Examiner	Group Art Unit

Invention:

METHOD AND APPARATUS FOR RAPID DATA TRANFER BETWEEN DIS-SIMILAR DEVICES

I hereby certify that the following correspondence:

New Patent Application Transmittal (& documents & fees listed as enclosed therein)

(Identify type of correspondence)

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to: The Assistant Commissioner for Patents, Washington, D.C. 20231 on

September 29, 2000
(Date)

James H. Walters
(Typed or Printed Name of Person Mailing Correspondence)

(Signature of Person Mailing Correspondence)

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APPLICATION INFORMATION

Title Line One:: METHOD AND APPARATUS FOR RAPID DATA TRAN
Title Line Two:: FER BETWEEN DIS-SIMILAR DEVICES
Total Drawing Sheets:: 2
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: F-316
Secrecy Order in Parent Appl.?:: No

REPRESENTATIVE INFORMATION

Representative Customer Number:: 802
Registration Number One:: 35731

Source:: PrintEFS Version 1.0.1

Express Mail #EL690074627US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Stan W. BOWLIN

S. N.

Filed: September 29, 2000

For METHOD AND APPARATUS FOR RAPID DATA TRANFER BETWEEN DIS-SIMILAR DEVICES

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please make the following amendments to this application prior to examination thereof:

In the Title:

Delete the title and substitute the following therefor:

--METHOD AND APPARATUS FOR RAPID DATA TRANSFER BETWEEN DIS-SIMILAR DEVICES--

REMARKS

The above amendment to the title is presented to correct a minor typographical error.

Respectfully submitted,

James H. Walters, Reg. No. 35,731

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DOCKET: F-316

METHOD AND APPARATUS FOR RAPID DATA TRANFER BETWEEN DIS-SIMILAR DEVICES

Background of the Invention

This invention relates to test instruments, and more particularly to a network test instrument.

In testing and analysis of networks, as network speeds increase, more efficient use of test instrument processing capabilities becomes important, to maximize analysis abilities and minimize hardware requirements. Therefore, it is desirable to move data on a bus only a single time, if possible. In network analysis instruments, various specialized processing chips may be employed, however, not all the desired devices in use in the instrument to which data may be destined behave similarly in receiving data. Thus, for example, at gigabit data transfer rates, there may not be sufficient time to employ multiple storing and retrieval of data to separate devices.

Summary of the Invention

In accordance with the invention, a method and apparatus is provided to transfer data between dis-similar devices.

Accordingly, it is an object of the present invention to provide an improved apparatus for minimizing the time to retrieve and store data in external memory and internal processor memory.

It is a further object of the present invention to provide an improved apparatus that stores data from a media access controller simultaneously in memory and in a DSP microprocessor.

The subject matter of the present invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. However,

both the organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with accompanying drawings wherein like reference characters refer to like elements.

Brief Description of the Drawings

FIG. 1 is a block diagram of a network test instrument embodying the invention; and

FIG. 2 is a timing diagram of operations according to the invention.

Detailed Description

The system according to a preferred embodiment of the present invention comprises a network test instrument adapted to speed operations by providing data from one source to two destinations substantially simultaneously.

Referring to FIG. 1, a block diagram of a network test device 10, the device connects to a network 12 via a media access controller (MAC) 14. The MAC is connected via a bus 16 to memory 18 (suitably SDRAM) and a digital signal processor (DSP) microprocessor 20. A complex programmable logic device (CPLD) 22 communicates to each of the MAC 14, the memory 18 and the DSP 20, providing control.

In operation, traffic from the network is received via the media access controller 14. The media access controller is a first-in first-out (FIFO) device and does not provide addressed access to or output for the data it receives. On the other hand, both the SDRAM 18 and the DSP microprocessor 20 employ addressing schemes for storage of data.

Typically, in accordance with the prior art, data received from the MAC would be read by the DSP via the

bus, and, if the data was to be stored, it would be written to the SDRAM via the bus by the DSP in a separate bus transfer operation. Therefore, the data would pass on the bus at least two separate times. In order to speed operations and not require that the microprocessor read the data from the media access controller and then, in a separate operation, write the data to memory, should it be decided that the data is to be stored in memory, in accordance with the present invention, when data is retrieved from the MAC, it is simultaneously written to a storage address in the SDRAM and into the DSP. Then, if the DSP determines that the data is to be saved, the address pointers to the memory are updated to select a next position in the memory for future data. However, if the DSP determines that the data is not to be stored in the memory, the address pointers are not updated, and instead remain set to the start point of the previous write to memory. That way, the next data that is provided from the MAC is written "over" the previous data that was not to be saved.

According to the invention, therefore, data received from the MAC need only pass the bus once, speeding operations.

The timing of the data transfer is accomplished by the CPLD via the control lines. A timing chart is illustrated in FIG. 2, wherein representative signals are illustrated.

Three signals from the DSP microprocessor are shown:

- Clock 24 (suitably a 60 MHz clock in the illustrated embodiment)
- DSP_Command 26 (command signal from the DSP µP)
- Trdsp_Addr 28 (address data supplied by the DSP to select row and column addresses of the SDRAM)

Two SDRAM signals are shown:

- Sdram_Command 30 (a command signal to direct the SDRAM operations)
- Row/Col Addr 32 (Row and Column selection data to address the SDRAM)

One signal from the MAC is shown:

- RX_Data 34 (received data from the MAC FIFO)

Referring still to FIG. 2, the timing of operations are controlled by CPLD 22. Therefore, when an indication that data is available in the FIFO of the MAC (for simplicity, that signal is not shown in the timing diagram), the DSP_Command line is set to ACTIVE during the last half of clock cycle 1 and the Trdsp_Addr is set to the ROW addressing location where data is to be written to in the memory, for a duration of one cycle. Shortly thereafter, at the beginning of clock cycle 2, the Sdram_Command line is set to ACTIVE and the Row/Col Addr line 32 is set to the ROW data for one cycle. Afterwards, Sdram_Command is set to NOP until a change at cycle 7. In the middle of clock cycle 4, (2 clock cycles after the end of the ROW data on the Trdsp_Addr line) the Dsp_Command is set to READ (indicating a read) and the Trdspp_Addr is set to carry the column selection COL indicating the column of memory to be selected in the SDRAM, both signals for 1 clock cycle duration. One half clock cycle later, at the beginning of clock cycle 5, the COL data is asserted on the Row/Col Addr line for 3 clocks. Soon after cycle 6 starts, the MAC RX_Data will begin on line 34 carrying the first word of data W1, the data W1 remaining until the end of cycle 7. At the start of cycle 7, Sdram_Command is set to WRITE for one clock. After Cycle 8 starts, Sdram_Command is set to NOP until

cycle 14. The RX_Data line will subsequently carry valid data from the MAC for next words W2, W3, W4, W5, W6 and W7 during the last half of clocks 9-13, respectively. During the last half of clock 11, a STOP command is set on Dsp_Command line 26. After the start of clock cycle 14, a STOP appears on Sdram_Command line 30, finishing the write to memory operation.

The timing control described hereinabove is accomplished by the CPLD 22, to provide timing signals and direct data to appear on the respective lines so that the SDRAM is provided the data according to the timing requirements it has, the MAC is able to write its data to the bus according to the timing requirements of the MAC, and the DSP is able to read the data under its timing requirements. Also, addressing, which is not provided by the MAC (since it is a FIFO device), is generated by the DSP and its timing of assertion is controlled by the CPLD. If, after the data transfer operation described herein, the DSP determines that the data is to be kept, then on the next write to the memory, the ROW and COLUMN addressing would be advanced to the next position in memory for storing data. However, if the data that had been written is not to be kept, then the next write operation will employ the same ROW and COLUMN addressing as the previous write, so that the previous data written to the SDRAM is discarded, as a result of being written over with new data.

The CPLD makes the decision of whether to perform the control operations to govern transfer of data from the MAC based on an address range to which the DSP makes read accesses. If the address is in a designated range, the data transfer as above is performed.

Therefore, in accordance with the invention, two or more destination devices are able to receive data

from a single source, substantially simultaneously. The devices may be dissimilar, such as a FIFO device not having an addressing scheme and memory or processor devices that do employ addressing. Further, while the bus cycles performed by the DSP, as the master device are read cycles, the SDRAM is operating as if performing write cycles. Transfer of the data from the MAC to both SDRAM and the DSP is thereby accomplished with a single bus transfer.

The system is preferably embodied in a network test instrument, and enables monitoring and processing of network data received through the MAC. Such received data is suitably analyzed and processed by the DSP to provide information and analysis of network operations.

While a preferred embodiment of the present invention has been shown and described, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from the invention in its broader aspects. The appended claims are therefore intended to cover all such changes and modifications as fall within the true spirit and scope of the invention.

Claims

What is claimed is:

1. A method for transferring data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:

supplying data from the source to first of said at least two destinations as a read data operation; and

supplying data to a second of said at least two destinations as a write operation.

2. The method according to claim 1, wherein the source comprises a non-addressed data device.

3. The method according to claim 2, wherein the source comprises a FIFO device.

4. The method according to claim 1, wherein at least one of the at least two destinations comprise addressed data devices.

5. The method according to claim 4, wherein the at least one destinations comprises a microprocessor.

6. The method according to claim 4, wherein the at least one destinations comprises a memory storage.

7. The method according to claim 4, wherein the at least one destinations comprises a SDRAM memory.

8. An apparatus for transferring received data from a network, comprising:

a bus;

a media access controller for putting the received data from the network onto said bus;

a microprocessor for reading the data from said bus;

a memory for writing the data from said bus into said memory; and

a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write the data to the bus, said memory write the data to said memory and said microprocessor read the data substantially simultaneously.

9. An apparatus for transferring data, comprising:

a bus;

a FIFO data source connected to said bus for putting data onto said bus;

a microprocessor connected to said bus for reading the data from said bus;

a memory connected to said bus for writing the data from said bus into said memory; and

a timing controller connected to said FIFO data source, said microprocessor and said memory for controlling said FIFO data source, said microprocessor and said memory to have said FIFO data source put the data onto the bus, said memory write the data to said memory and said microprocessor read the data substantially simultaneously.

Abstract of the Disclosure

A system for transferring data from one source to plural destination devices, employs timing and bus signal control to have one destination device treat the transfer as a read operation, while another destination device treats the transfer as a write operation.

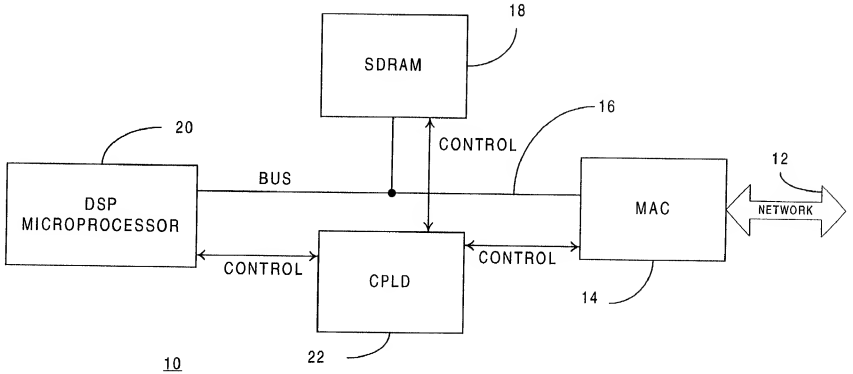
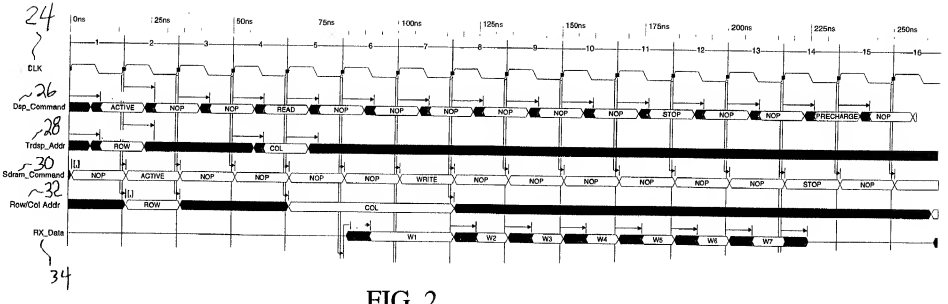


FIG. 1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200ns
225ns
250ns
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7
8
9
10
11
12
13
14
15
16
CLK
26
Dsp_Command
ACTIVE
NOP
READ
STOP
PRECHARGE
28
Trdsp_Addr
ROW
COL
30
Sdram_Command
WRITE
32
Row/Col Addr
RX_Data
W1
W2
W3
W4
W5
W6
W7
34

FIG. 2

Docket No.
F-316

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR RAPID DATA TRANFER BETWEEN DIS-SIMILAR DEVICES

the specification of which

(check one)

☒ is attached hereto.

☐ was filed on _____ _____ as United States Application No. or PCT International Application Number _____

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 385(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

James H. Walters, Reg. No. 35,731
G. Thomas Noe, Reg. No. 26,967

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Direct Telephone Calls to: *(name and telephone number)*
James H. Walters 503-224-0115

Full name of sole or first inventor
Stan W. Bowlin

Sole or first inventor's signature Stan W. Bowlin Date 9-29-00

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Second inventor's signature Date

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Citizenship

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